Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) Component with a dynamically reconfigurable architecture for processing data comprising a data processing block TD and a general controller CG capable of controlling the data processing block TD characterized in that:

   - the block TD comprises a plurality of reconfigurable elementary data processing blocks BE; each elementary block BE comprises two inputs, E1 and E2 for reception of data to be processed, and one output S for transmission of processed data; a common input data bus being capable of transmitting data to be processed to the input E1 of each of the blocks BE and the controller CG; for each block BE, an output data bus connected to its output S, being capable of transmitting processed data outside the component and through a bypass data bus to the input E2 of a single other block BE;
   - the controller CG is capable of initializing configurations of blocks BE and controlling their dynamic reconfiguration, controlling data flows at the output from each block BE so as to transmit data either towards the outside or to the input E2 of another block BE, and controlling data flows at the input of each block BE.

2. (Original) Component according to claim 1 in which the controller CG is capable of controlling transmission of data received from the outside on the common input data bus as and when they arrive, in sequence to each of the blocks BE, the data being transmitted to the next block BE when the maximum processing capacity of the previous block BE is reached.

3. (Currently Amended) Component according to claim 1 in which the controller CG is capable of initializing the ~~les~~ configurations of blocks BE block by block, and controlling the dynamic reconfiguration of blocks, block by block, so as to make the block TD capable of processing data in pipeline mode or in parallel mode or in combined mode.

4. (Original) Component according to claim 3 in which:

- each block BE in the block TD comprises a plurality of configurable data processing units UT and corresponds to a row in a matrix network of units UT in the block TD; the units UT in each pair of successive units in each block BE being capable of exchanging data through an associated configurable two-directional communication block BCOM dedicated to these two units;
- the input unit UT for each block BE that corresponds to the first unit UT on the row corresponding to the block, is capable of receiving data received on inputs E1 or E2 of the block as input, and the output unit UT from the block that corresponds to the last unit UT on the row corresponding to the block, is capable of transmitting data processed at the output S from the block as output;
- for each block BE, the controller CG is capable of receiving instructions from the outside for processing data by each unit UT in the block and memorizing these data, initializing configurations for each unit UT and for each block BCOM in the block BE and controlling their dynamic reconfiguration.

5. (Original) Component according to claim 4 in which:

- blocks BCOM in each pair of blocks BCOM, for which the associated units UT are on adjacent columns and adjacent rows in the matrix network of units in block TD, and are

capable of exchanging data through an associated inter-row register REG so as to enable data to be exchanged between units UT from one row to the next;

- the controller CG is capable of controlling the dynamic reconfiguration of units UT and blocks BCOM of the block TD to make the block TD capable of processing data in dependent rows mode, for at least two adjacent rows in the matrix network, by controlling switching of data between two blocks BE corresponding to two adjacent rows, through an inter-row register REG between these two rows.

6. (Original) Component according to claim 5 in which the controller CG is capable of transmitting RESET or ENABLE type or clock signals through a control bus to each register REG in the block TD, and in which each inter-row register REG between two blocks BCOM is capable of:

- storing data received from a block BCOM in a memory and making the data available for the other block BCOM;
- receiving RESET or ENABLE or clock type signals sent by the controller CG and executing commands corresponding to these signals.

7. (Original) Component according to claim 6 in which the inputs E1 and E2 of a block BE are the inputs of a multiplexer associated with the block, the output from the multiplexer being connected to the input of the input unit UT of the block BE for transmission of data to this unit.

8. (Original) Component according to claim 7 in which the data processing units UT of block TD are banks of configurable synchronous elementary data processing cells CE, each bank

comprising at least one elementary cell CE; the cells CE in any unit UT of any block BE are connected to a common control bus that connects them to the controller CG, the controller CG being capable of controlling cells CE and controlling their reconfiguration; for each pair of adjacent units UT in a block BE, the elementary cells of a unit UT are capable of exchanging data with the elementary cells in the other unit UT through the block BCOM associated with these units, the block BCOM being capable of making these data exchanges; each cell CE in the input unit UT of each block BE, that corresponds to the first unit UT on the row corresponding to the block, is capable of receiving data received at the input of the unit UT as input through a data bus common to every cell CE in the unit UT; each cell CE in the unit UT output from each block BE, corresponding to the last unit UT on the row corresponding to the block, is capable of transmitting data to the output S from the block through a data bus common to every cell CE in the unit UT, as output.

9. (Original) Component according to claim 8 in which each block BCOM associated with units UT comprises:

- a transmission block BT capable of exchanging data between elementary cells CE in a unit UT and the cells CE in another unit UT with which the BCOM is associated; the block BT being configurable by a local block controller CLB;
- a local block controller CLB capable of receiving and interpreting control signals from the controller CG and configuring the block BT, according to configuration data received and stored in a local configuration memory MB, for data transmission; the controller CLB being capable of managing loading into memory MB as a function of control signals received from the controller CG;
- a general controller CG capable of controlling local controllers CLB of the block TD.

10. (Previously Presented) Component according to claim 8 in which each synchronous elementary cell CE in a bank comprises:

- an operator block BO capable of receiving input data through an input data bus, storing them and performing processing on these data according to configuration signals originating from a local cell controller CLC; transmitting the result of the processing to the output through an output data bus;
- a local cell controller CLC capable of:
- receiving data through the input data bus;
- managing different operating modes of the cell CE, in other words an initialization mode, to load cell configuration words into a local configuration memory MC, a test mode to perform structural tests on the cell, and a normal mode for execution of data processing operations as a function of configuration signals emitted by the controller CG and received by the local controller through the common control bus;
- managing loading into memory MC as a function of a cell operating mode indicated by the controller CG;
- interpreting configuration signals received from the controller CG to either load a corresponding configuration word into a local configuration register RCL to maintain it throughout the data processing cycle by the cell, or to configure the block BO as a function of a configuration word appearing in the register RCL;
- perform structural tests of the cell CE on reception of a test mode signal sent by the controller CG;

- a general controller CG capable of controlling the local controllers CLC of the block TD.

11. (Original) Component according to claim 10 in which the local cell controller CLC is capable of interpreting configuration signals received from the controller CG so as to firstly read a cell configuration number on the common control bus and then load a configuration word locally corresponding to this number, according to a local correspondence table, in the RCL register; cell configuration numbers being stored in a controller memory CG and the controller CLC being capable of memorizing the local correspondence table.

12. (Previously Presented) Component according to claim 10 in which the controller CG is capable of receiving a malfunction indication resulting from a structural test applied to a cell CE, from this cell, and sending a command to the local controller CLC of the cell CE to configure this cell in BYPASS mode.

13. (Previously Presented) Component according to claim 9 in which the local block controller CLB of a communication block BCOM, connected to a unit UT, is capable of configuring the block BCOM in BYPASS mode when the controller CG, having received a malfunction indication from one or several cells CE of the unit UT, transmits a signal to force a change to BYPASS mode to the controller CLB. The controller CG being capable of controlling a changeover of a block BCOM of a unit UT to BYPASS mode when a command to configure a cell CE of the unit UT into BYPASS mode has been transmitted to the local controller CLC of the cell CE.

14. (Previously Presented) Component according to claim 8 in which the result of data processing done by a cell CE can be stored in a local register; a result stored in this local register being maintained during reconfiguration of the cell.

15. (Previously Presented) Component according to claim 1 comprising:

- an input management block GE capable of receiving data from the outside and temporarily storing these received data, formatting stored data according to the initialization mode or normal mode indicated by the controller CG through a specific control bus, transmitting formatted data to the input E1 of blocks BE of the block TD through the common input data bus;
- an output management GS block connected to the controller CG through a specific control bus for controlling reception of processed data, connected to the output data bus from each of the blocks BE in the block TD to receive processed data, and capable of reformatting the received processed data, storing the reformatted data in a buffer memory, receiving a transmission request from the outside, transmitting data stored in the buffer memory to the outside following a request received from the outside.

16. (Previously Presented) Component according to claim 10 in which the local controller CLC of cell CE, the local controller CLB of block BCOM and the general controller CG are capable of using a JTAG method to load configurations during the dynamic component reconfiguration phase, and to perform tests; the controller CG comprising a TAP controller connected through JTAG serial buses, block BE by block BE, to cells CE and blocks BCOM in block TD.

17. (Previously Presented) Component according to claim 4 in which there is an even number N of units UT on network rows and the blocks BCOM are distributed in N/2 basic cells CB, each cell CB comprising two adjacent units UT and the block BCOM associated with these units; the controller CG being capable of controlling dynamic reconfiguration of cells CB in the network and communication blocks BCOM between cells CB, row by row, to make the block TD capable of processing data using cells CB.

18. (Original) Component according to claim 17, for processing of a set of applications comprising at least one application, in which each basic cell CB in the block TD configured to perform processing can perform the operations necessary for complete processing of at least one application of the assembly, each application of the assembly possibly being done completely by at least one basic cell CB.